Investigation of MUX Using Various CMOS Circuit Style under Nanometer Technology

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Received 1 April` 2019 Received in revised form 20 April 2019 Accepted 21 April 2019
Available online 26 April 2019

Abstract— **Since multiplexer (MUX) is one of the important components of communication system, to increase the efficiency of data transmission, to utilize the vast memory space of a computer in an effective way and to convert parallel form of data into serial form in telecommunication networks an efficient design of low power -delay MUX is required. Hence in this work, a basic 2:1 MUX is designed using various CMOS logic families such as Static CMOS logic, Pseudo NMOS logic, Domino logic and Dual-Rail Domino logic to identify the best logic family suitable for the design of higher levels of MUX. The implementation is done in VLSI technology as it has features like small size, low cost, high operating speed and low power. The performance analysis of the MUX using various CMOS logic families are conducted using VLSI back- hand tool: CADENCE VIRTUOSO SCHEMATIC EDITOR 6.1 at 180nm.The results obtained show that, the Domino logic based 2:1 MUX is the most efficient design because the average power consumption is 20.06% and PDP(Power Delay Product) is 20.1% lesser than that of other logic familes. But trade-offs are inferred between Domino logic and Static CMOS logic which can be neglected on considering the overall performance. Since the Domino logic outperforms the other logic families, this work suggests that any higher level MUX with low power-delay and PDP can be achieved using Domino logic.**

***Keywords*—MUX, CMOS logic, Pseudo NMOS logic, Domino logic , Dual-Rail Domino logic , power-delay and CADENCE**

I. INTRODUCTION

MUX is a **data selector** that selects one of several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2 ^{n} inputs has *n* select lines, which are used to select which input line to send to the output2:1 MUX is a basic block of the "switch logic" [9].It has two input lines D0 and D1, one select line S and one output lone Y[6] as shown in Fig 1. The truth table of 2:1 MUX is given in Table I; the logic function is

$$Y = \bar{S} \cdot D0 + S \cdot D1$$

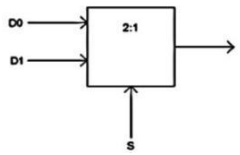

Figure 1. Symbol of 2:1 MUX

TABLE I. TRUTH TABLE OF 2:1 MUX

SELECT LINE	INPUT		OUTPUT
~S/S	D1	D0	Y
1/0	X	0	0
1/0	X	1	1
0/1	0	X	0
0/1	1	X	1

There are two types of CMOS logic families such as static and dynamic circuits.

Static CMOS circuit is shown in Fig.2 are used in various logic gates in integrated circuits. These are designed with complementary nMOS Pull-Down Network (PDN) and pMOS Pull-Up Networks (PUN). They have simple design; hence they are insensitive to variations, good noise margins, fast operating speed and low power. Nevertheless, performance or area constraints occasionally dictate the need for other circuit families and the most important alternative is dynamic circuits.

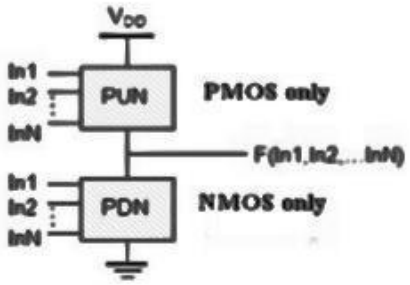

Figure 2.CMOS Static Logic

Dynamic circuit shown in Fig.3 uses simple sequential circuits along with memory functions. It is dependent on temporary storage of charges in parasitic node capacitance. Dynamic circuits require less silicon area and have superior performance over conventional Static Logic circuits [4]. Thus these circuits have gained a widespread use .It also uses a sequence of Precharge and Evaluation Phases governed by the clock to recognize complex logic functions.

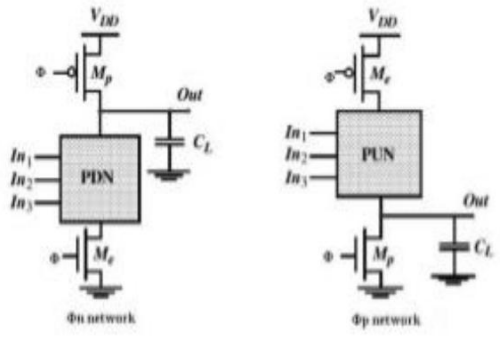

Figure 3. CMOS Dynamic Logic

Precharge Phase

When clock signal (Φ) = 0, the output node Out is precharged to VDD by the PMOS transistor Mp and the evaluate NMOS transistor remains off, so that the pull-down path is disabled.

Evaluation Phase

In the PDN when clock signal (Φ) = 1, the pre -charge transistor Mp is OFF, and the evaluation transistor M_e is turned ON.

Both the circuit families have different types of logics. Considering the above mentioned features, static CMOS logic and pseudo NMOS are chosen from static circuits and Domino and Dual Rail logic are selected from dynamic circuits, for the implementation of a MUX. There is wide scope for research in the field of CMOS logic families in spite of many designs proposed till date [5].

Very-large-scale integration (VLSI) is the technology that provides a platform in designing a complex circuitry even with millions of transistors in an extremely small space on a single chip known as Integrated circuit (IC) [9]. Reduced size, fast operating speed, high reliability and reduced area are the advantages of VLSI. Thus this entire work is implemented using a VLSI back-end tool, to determine the performance metrics of various CMOS logic families.

II. Proposed Work

A. Design of efficient MUX

In this work, the 2:1 multiplexer has been designed using various logic families such as Static CMOS logic, Pseudo NMOS logic, Domino logic and Dual Rail Domino logic as shown in Fig.4. The transistor sizing for the 2:1 MUX designed using the above logics is shown is Table II.

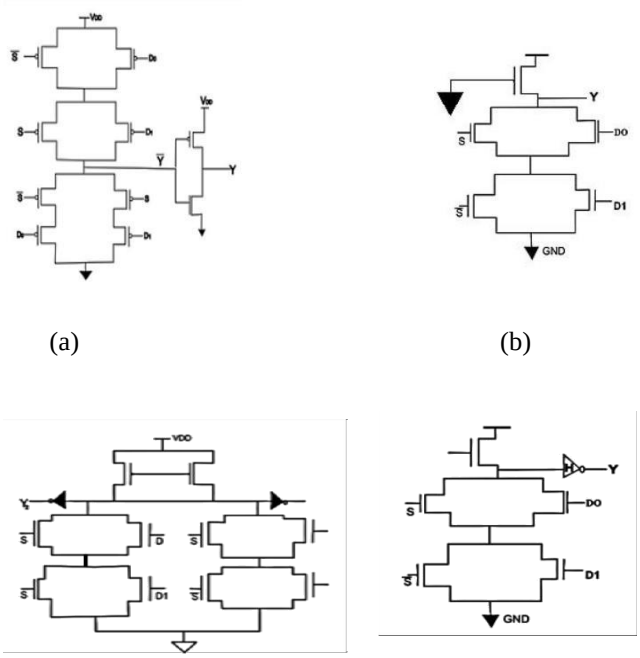

Figure 4. Design of 2:1 MUX using (a) Static CMOS (b) Pseudo logic (c) Dual Rail Domino logic (d) Domino logic

Static CMOS Logic is constructed with the help of a PUN and a PDN as shown in Fig. 4(a). The function of the PDN is to provide a connection between the output and VDD when the output of the logic gate is supposed to be 1. Similarly, the PDN connects the output to ground when the output is expected to be 0. The PUN and PDN networks are constructed in a mutually exclusive manner such that either PDN or PUN is conducting in steady state. One of the major advantages of Static CMOS logic is that they have zero quiescent power dissipation, where for any applied input state either the PUN or the PDN remains off. The problem with this type of implementation is that more area is required in implementing logics. This has an impact on the capacitance and thus the speed of the gate [1].

In **Pseudo NMOS Logic** the PDN is like that of an ordinary static gate, but the PUN has been replaced with a single pMOS transistor that is grounded so it is always ON as in Fig. 4(b). The pMOS transistor widths are selected to be about 1/4 the strength (i.e., 1/2 the effective width) of the nMOS PDN as a compromise between noise margin and speed; this best size is process-dependent [1]. In this way the area required to implement logics have been reduced which in turn increases the speed. But these Pseudo NMOS logics have various other drawbacks such as slow rising transitions, contention on the falling transitions, static power dissipation.

Dynamic Logics circumvent the drawbacks of Pseudo NMOS by using a clocked PUN rather than a pMOS that is always ON. But the main issue in Dynamic logic compared to Static CMOS logic, is the monotonicity requirement. During an evaluation phase of dynamic gate the inputs must be monotonically raising for the dynamic gate to compute the

correct function [1].To overcome this monotonicity problem Domino logic was used.

Domino Logic was introduced to overcome the monotonicity problem faced the Dynamic logic circuits. The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates, as shown in Fig 4(d). This converts the monotonically falling output into a monotonically rising signal suitable for the next gate [1].

The name Domino comes from the behavior of a chain of the logic gates. It runs 1.5-2 times faster than static logic circuits. It is simply a logic which permits high-speed operation and enables the implementation of complex functions which otherwise is not achieved by Static and Dynamic circuits [1],[2].

Domino logic offers a simple technique to eliminate the need of complex clocking scheme by utilizing a single phase clock and have no static power consumption as it is removed by clock input in the first stage. These logic circuits are glitch free, have fast switching threshold and possibility to cascade [7].

Dual-Rail Domino a complete logic family in that it can compute all inverting and non-inverting logic function which is a drawback in Domino Logic as it can implement only inverting logic. However, it requires more area, wiring, and power.

TABLE II. TRANSISTOR SIZING FOR 2:1 MUX

LOGIC FAMILIES	NUMBER OF TRANSISTORS	AREA WIDTH (m)
Static CMOS	12	4.32p
Pseudo NMOS	7	2.52p
Domino logic	7	2.52p
Dual-Rail Domino	14	5.04p

From Table II, it can be inferred that Pseudo NMOS and Domino logic has minimum transistor count and area. Hence to verify this experimentally, VLSI back-end tool CADENCE VIRUOSO SCHEMATIC EDITOR is used for implementing various CMOS logic families and to analyze their performance.

III. Simulation Results And Discussion

A.Simulation Environment

The entire work has been implemented using the back -end tool Cadence 6.1 virtuoso which is supported by Red Hat Enterprise (Linux) operating system. It works under 180nm with an operating frequency of 2.8GHz.

B. Performance metrics

In this work the optimum design of MUX is identified experimentally by comparing the various performance metrics such as **average** power, static power, dynamic power and propagation delay.

Average Power is characterized as the power consumed by the circuit so as to give the output. By reducing the power supply from the circuit automatically the power consumed by the circuit will be reduced.

Unit: watt (W).

$$Average\ power = Static\ power + Dynamic\ Power \quad (1)$$

Propagation delay is the time required for a digital signal to travel from the input of a logic gate to the output switch.

Unit: seconds (s)

$$Delay = \frac{T(rf)+T(fr)}{2} \quad (2)$$

Where, T(rf) is the rise time, T(fr) is the fall time

Area is the product of length, width and the number of transistors used to implement a circuit. It gives the amount of silicon area needed to implement a circuit.

Unit: square meter (m^2)

$$\mathbf{Area = L * W * (No.\ of\ transistors\ required)} \quad (3)$$

Where, **L** is the length, **W** is the width

Power delay product (PDP) is the product of the average power and the delay of the circuit. **Unit:** joules (J)

$$PDP = Average\ power * Delay \quad (4)$$

C. Static CMOS Logic

The static CMOS based 2:1 MUX has been designed using a PUN consisting of 4 pMOS and a PDN consisting of 4 nMOS. The PUN is constructed using two parallel pMOS circuits connected in series. The PDN is constructed using two series nMOS circuits connected in parallel. The output of the Static CMOS logic is connected to an inverter to obtain the correct output. VDD is connected to the pull-up circuit to provide power supply and the ground is connected to the pull-down circuit. The inputs to the circuit is provided with the help of V_{pulse} which is set according the truth table of 2:1 MUX. The schematic of static CMOS logic is shown in Fig.5 and its test bench waveform is shown in Fig.9.

D. Pseudo NMOS Logic

The design of 2:1 MUX using Pseudo NMOS logic is similar to Static CMOS logic except that the entire PUN is replaced by a single pMOS transistor and grounded permanently to reduce the transistor count. The output of the Pseudo NMOS is connected to an inverter to obtain the correct output as shown in Fig.6 and its test bench waveform is shown in Fig.10. The power supply is provided through VDD connected to the pull-up circuit and the circuit inputs are given with the help of V_{pulse} as per the truth table of 2:1 MUX.

Name of the logic	No of transistors	Average power(W)	Delay (s)	Power Delay Produce (PDP) (J)	Area (m)
Static CMOS	12	55.33µ	4.573n	0.253	4.32p
Pseudo NMOS	7	411.5µ	4.561n	1.87	2.52p
Domino logic	**7**	**126.2µ**	**4.5505n**	**0.574**	**2.52p**
Dual Rail domino	14	248.8µ	4.5515n	1.13	5.04p

E. Domino Logic

The construction of 2:1 MUX using Domino logic is just as same as that of the Pseudo NMOS logic. The only difference is that the PUN that has been grounded is supplied with a high clock skew which is provided by the V_{pulse}. The output is connected to a CMOS inverter to overcome monotonicity problem and to improve the circuit performance as shown in the Fig.7. VDD is used to provide the power supply to the circuit connected to the pull-up circuit and the other inputs provided through V_{pulse}. The test bench waveform of the Domino logic is shown in Fig.11.

F. Dual Rail Domino Logic

The 2:1 MUX using Dual Rail Domino logic is designed by connecting complimentary domino logic with the actual domino logic as shown in Fig.10. All the other working principles remain same as that of the Domino logic.
The output test bench waveform of the Dual Rail Domino logic is shown in Fig.12.

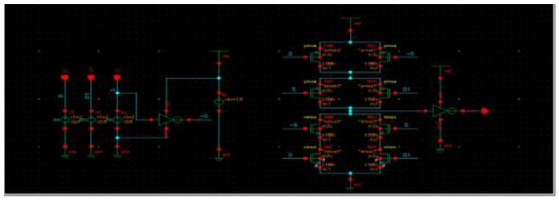

Figure 5. Schematic of Static CMOS logic

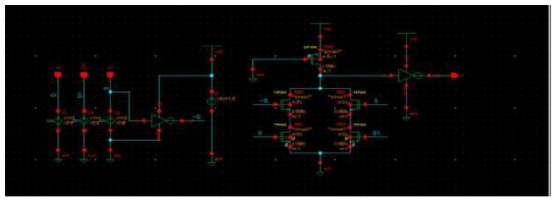

Figure 6. Schematic of Pseudo NMOS logic

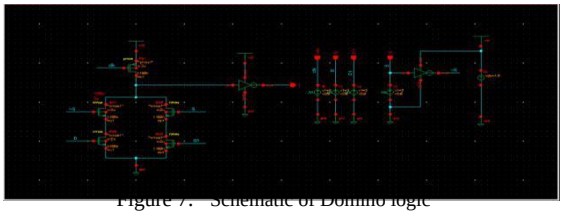

Figure 7. Schematic of Domino logic

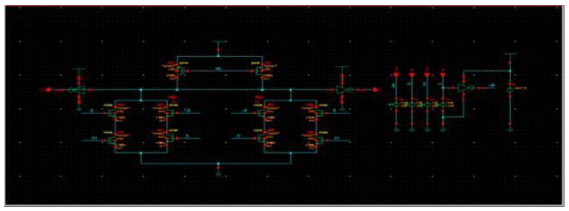

Figure 8.Schematic of Dual-Rail Domino logic

TABLE III. PERFORMANCE ANALYSIS OF 2:1 MUX USING VARIOUS CMOS LOGIC FAMILIES

Table III depicts that the domino logic has minimum average power consumption compared to the other logics except for static CMOS which has 56.15% decrease in power consumption than the Domino logic. There is also reduction in PDP by 20.1% compared to all logics except for CMOS logic. Hence there is trade-off between Static CMOS and Domino logic, but the results obtained prove that the Domino logic has an overall better performance.

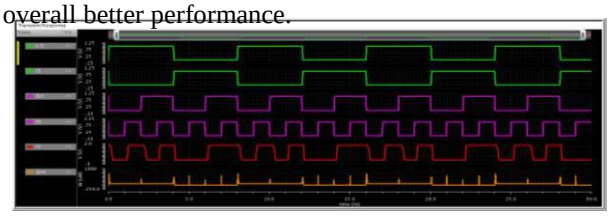

Figure 9. Test bench waveform of Static CMOS logic

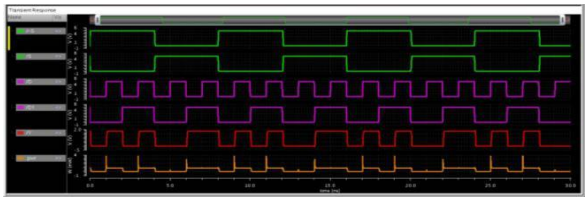

Figure 10. Test bench waveform of Pseudo NMOS logic

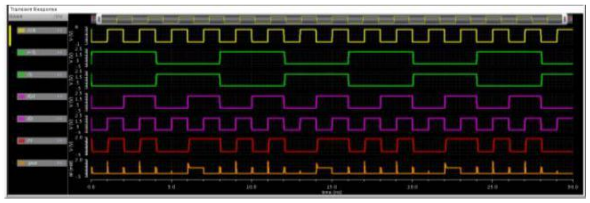

Figure 11. Test bench waveform of Domino logic

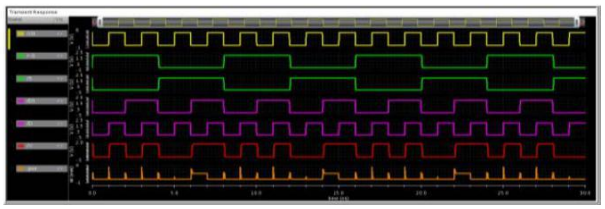

Figure 12. Test bench waveform of Dual-Rail Domino logic

D,D1 -select lines ; **~S,S**-select lines; **Y**- output **pwr**-average power**;** **clk**- clock input

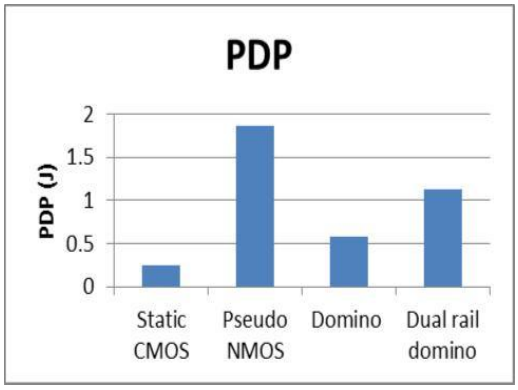

Figure 13. PDP Analysis of various CMOS Logic Families

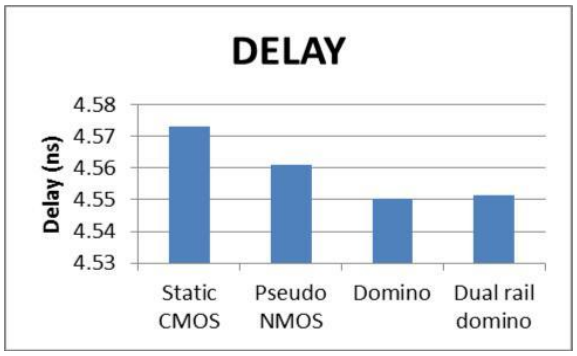

Figure 14. Delay Analysis of various CMOS Logic Families

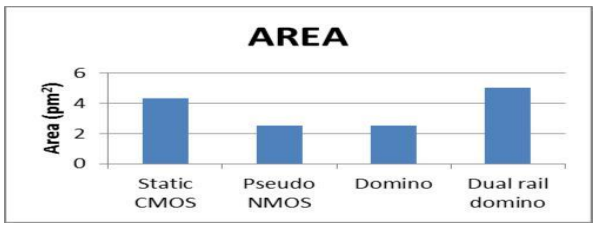

Figure 15. Area Analysis of various CMOS Logic Families

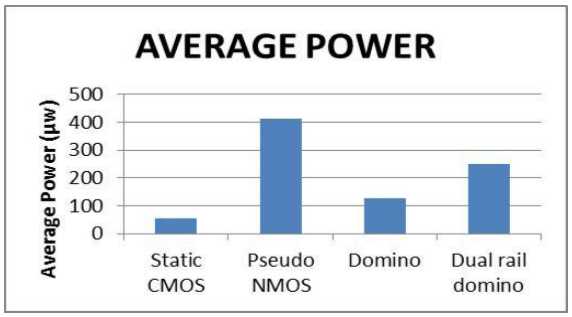

Figure 16. Average Power Analysis of various CMOS Logic Families

The performance metrics of various CMOS logic families are analyzed as shown in Fig 13 through Fig 16. From Fig. 13 showing the PDP (Power Delay Product) of various logic families, it is inferred that Static CMOS logic has the minimum power, similarly Fig.16 shows the comparison between Average power of various logic families which also depicts that Static CMOS logic has minimum power comsumption. But considerig the Dealy and Area the 2:1 MUX designed using Domino logic out performs the other logic families as shown in Fig.14 and Fig.15. Thus the performance analysis proves that the overall performance of 2:1 MUX designed using Domino logic to be most efficient.

Conclusion

In this paper, a 2:1 MUX is implemented using various CMOS logic families and it's performance metrics are analyzed. It is clearly inferred that, 2:1 MUX designed using domino logic is the most efficient design because the reduction in average power consumption is 20.06% and in PDP is 20.1% compared to all the other logic familes and the propagation delay is also lesser, but there are trade-off between Domino logic and Static CMOS logic which can be neglected on considering the overall performance. Thus the overall analysis proves that power and delay efficient MUX can be designed using the domino logic which out performs all the other logic families. The significance of a Multiplexer is that it can be used in Parallel to Serial convertor (which a major application of MUX) to reduce wide parallel busses to serial signals in the field of Telecommunication, Data communication, Satellite and Military applications. Therefore, based on all the performance analysis made in this work it is proved that MUX designed using Dominologic can be used in various applications to obtain better performance.

ACKNOWLEDGMENT

We would like to thank St. Joseph's College of Engineering, Chennai, which provided us with the cadence virtuoso tool and working at 180nm.

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